REMARKS

Applicants respectfully request reconsideration of the present U.S. patent application. Claims 1-22 stand rejected under 35 U.S.C. § 103. Claims 1 and 13 have been amended. No claims have been canceled or added. Therefore, claims 1-22 remain pending.

Claim Rejections - 35 U.S.C. § 103

Rejections of Claims 1, 3, 6-14, 16, 17 and 20-22 based on *Taniguchi* and *Holt*

Claims 1, 3, 6-14, 16, 17 and 20-22 were rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 5,162,756 issued to Taniguchi et al. (*Taniguchi*) in view of Electronic Circuits – Digital and Analog by Holt (*Holt*). For at least the reasons set forth below, Applicants submit that claims 1, 3, 6-14, 16, 17 and 20-22 are not rendered obvious by *Taniguchi* in view of *Holt*.

Claim 1 recites the following:

> a first amplifier configured to receive an input signal, and in response, provide a first output signal;
> a first delay circuit configured to introduce a first delay to the input signal, thereby creating a delayed input signal, wherein the delayed input signal is delayed relative to the input signal received by the first amplifier;
> a second amplifier configured to receive the delayed input signal, and in response, provide a first delayed output signal; ...

Claim 13 is a method claim, and recites similar limitations.

Taniguchi discloses a high frequency signal power divider/combiner. See Fig. 2; col. 3, lines 7-16 and 55-56. The power divider/combiner includes six transmission lines (L_1-L_6) having lengths of one-quarter of the wavelength of the frequency of the signal passing through the transmission lines. See Fig. 2; col. 3, lines 17-23 and 37-38. In addition, the power divider/combiner uses four high frequency amplifiers (FETs) to

amplify a high frequency input signal and obtain a high power, high frequency output signal. See Fig. 2; col. 3, lines 55-59; col. 9, lines 16-18.

Examiner notes that the first amplifier in *Taniguchi* receives a signal through transmission line L_3. See Office Action, page 2, lines 13-15. Moreover, according to the Examiner, transmission line L_4 of *Taniguchi* is "a first delay element that introduces a delay to the input signal and applies this to the input of a 'second' amplifier FET_2." See Office Action, page 2, lines 17-18.

As set forth above, transmission lines L_3 and L_4 in *Taniguchi* are both one-quarter wavelength transmission lines. Therefore, if Examiner believes transmission line L_4 is a delay element, then Examiner must believe that transmission line L_3 is a delay element. Consequently, based on Examiner's interpretation, *Taniguchi* discloses two FETs that are each receiving a delayed input signal. As a result, *Taniguchi* does not disclose a first amplifier configured to receive an input signal, and in response, provide a first output signal, a first delay circuit configured to introduce a first delay to the input signal, thereby creating a delayed input signal, wherein the delayed input signal is delayed relative to the input signal received by the first amplifier, and a second amplifier configured to receive the delayed input signal, and in response, provide a first delayed output signal, as recited in claims 1 and 13. Thus, *Taniguchi* fails to disclose at least one limitation of claims 1 and 13.

Examiner cites *Holt* for the proposition that it would have been obvious "to provide *Taniguchi* with a bias control circuit(s) that biases the first and second amplifiers such that linear operation is obtained for these amplifiers." See Office Action, page 3, lines 28-30. Examiner does not assert that *Holt* discloses a first amplifier configured to receive an input signal, and in response, provide a first output signal, a first delay circuit

configured to introduce a first delay to the input signal, thereby creating a delayed input signal, wherein the delayed input signal is delayed relative to the input signal received by the first amplifier, and a second amplifier configured to receive the delayed input signal, and in response, provide a first delayed output signal.

Therefore, regardless of whether Examiner is correct regarding *Holt*, *Holt* fails to cure the deficiencies of *Taniguchi* pointed out by Applicants. Thus, *Taniguchi* in view of *Holt* fails to disclose at least one limitation of claims 1 and 13. Consequently, claims 1 and 13 are not rendered obvious by *Taniguchi* in view of *Holt* for at least the reasons set forth above. Applicants therefore respectfully request that the Examiner withdraw the rejections of claims 1 and 13 under 35 U.S.C. § 103.

Claims 3 and 6-12 depend from claim 1. Claims 14, 16, 17 and 20-22 depend from claim 13. Because dependent claims include the limitations of the claims from which they depend, Applicants submit that claims 3, 6-12, 14, 16, 17 and 20-22 are not rendered obvious by *Taniguchi* in view of *Holt* for at least the reasons set forth above.

Rejections of Claims 4, 5, 18 and 19 based on *Taniguchi*, *Holt* and *Kim*

Claims 4, 5, 18 and 19 were rejected under 35 U.S.C. § 103 as being unpatentable over *Taniguchi* in view of *Holt*, and further in view of U.S. Patent No. 6,617,929 issued to Kim et al. (*Kim*). For at least the reasons set forth below, Applicants submit that claims 4, 5, 18 and 19 are not rendered obvious by *Taniguchi* in view of *Holt* and *Kim*.

As explained above, *Taniguchi* in view of *Holt* fails to disclose a first amplifier configured to receive an input signal, and in response, provide a first output signal, a first delay circuit configured to introduce a first delay to the input signal, thereby creating a delayed input signal, wherein the delayed input signal is delayed relative to the input

signal received by the first amplifier, and a second amplifier configured to receive the delayed input signal, as recited in claims 1 and 13.

Examiner cites *Kim* with regard to impedance matching circuits. See Office Action, page 4, lines 19-27. Examiner does not assert that *Kim* discloses a first amplifier configured to receive an input signal, and in response, provide a first output signal, a first delay circuit configured to introduce a first delay to the input signal, thereby creating a delayed input signal, wherein the delayed input signal is delayed relative to the input signal received by the first amplifier, and a second amplifier configured to receive the delayed input signal. Therefore, regardless of whether Examiner is correct regarding *Kim*, *Kim* fails to cure the deficiencies of *Taniguchi* in view of *Holt* pointed out by Applicants. Thus, *Taniguchi* in view of *Holt* and *Kim* fails to disclose at least one limitation of claims 1 and 13. Consequently, claims 1 and 13 are not rendered obvious by *Taniguchi* in view of *Holt* and *Kim* for at least the reasons set forth above.

Claims 4 and 5 depend from claim 1. Claims 18 and 19 depend from claim 13. Because dependent claims include the limitations of the claims from which they depend, Applicants submit that claims 4, 5, 18 and 19 are not rendered obvious by *Taniguchi* in view of *Holt* and *Kim* for at least the reasons set forth above. Applicants therefore respectfully request that the Examiner withdraw the rejections of claims 4, 5, 18 and 19 under 35 U.S.C. § 103.

Rejections of Claims 2 and 15 based on *Taniguchi*, *Holt* and *Cheng*

Claims 2 and 15 were rejected under 35 U.S.C. § 103 as being unpatentable over *Taniguchi* in view of *Holt*, and further in view of Cheng et al., U.S. Patent Application

No. 2002/0190790 (*Cheng*). For at least the reasons set forth below, Applicants submit that claims 2 and 15 are not rendered obvious by *Taniguchi* in view of *Holt* and *Cheng*.

As explained above, *Taniguchi* in view of *Holt* fails to disclose a first amplifier configured to receive an input signal, and in response, provide a first output signal, a first delay circuit configured to introduce a first delay to the input signal, thereby creating a delayed input signal, wherein the delayed input signal is delayed relative to the input signal received by the first amplifier, and a second amplifier configured to receive the delayed input signal, and in response, provide a first delayed output signal, as recited in claims 1 and 13.

Examiner cites *Cheung* with regard to selectively supplying bias voltages. See Office Action, page 5, lines 1-7. Examiner does not assert that *Cheng* discloses a first amplifier configured to receive an input signal, and in response, provide a first output signal, a first delay circuit configured to introduce a first delay to the input signal, thereby creating a delayed input signal, wherein the delayed input signal is delayed relative to the input signal received by the first amplifier, and a second amplifier configured to receive the delayed input signal. Therefore, regardless of whether Examiner is correct regarding *Cheung*, *Cheung* fails to cure the deficiencies of *Taniguchi* in view of *Holt* pointed out by Applicants. Thus, *Taniguchi* in view of *Holt* and *Cheung* fails to disclose at least one limitation of claims 1 and 13. Consequently, claims 1 and 13 are not rendered obvious by *Taniguchi* in view of *Holt* and *Cheung* for at least the reasons set forth above.

Claim 2 depends from claim 1. Claim 15 depends from claim 13. Because dependent claims include the limitations of the claims from which they depend, Applicants submit that claims 2 and 15 are not rendered obvious by *Taniguchi* in view of

Holt and *Cheng* for at least the reasons set forth above. Applicants therefore respectfully request that the Examiner withdraw the rejections of claims 2 and 15 under 35 U.S.C. § 103.

CONCLUSION

For at least the foregoing reasons, Applicants submit that the rejections have been overcome. Therefore, claims 1-22 are in condition for allowance and such action is respectfully solicited. The Examiner is respectfully requested to contact the undersigned by telephone if such contact would further the examination of the present application.

Respectfully submitted,

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